IF-TH-60

Coupling Between Microstrip Lines With Finite Width Ground Plane Embedded in Polyimide Layers for 3D-MMICs on Si

George E. Ponchak[1], Edan Dalton[2], Emmanouil M. Tentzeris[2], and John Papapolymerou[2]

1. NASA Glenn Research Center, Cleveland, OH 44135
2. School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332-0250

Abstract — **Three-dimensional circuits built upon multiple layers of polyimide are required for constructing Si/SiGe monolithic microwave/millimeter-wave integrated circuits on CMOS (low resistivity) Si wafers. Thin film microstrip lines (TFMS) with finite width ground planes embedded in the polyimide are often used. However, the closely spaced TFMS lines are susceptible to high levels of coupling, which degrades circuit performance. In this paper, Finite Difference Time Domain (FDTD) analysis and experimental measurements are used to show that the ground planes must be connected by via holes to reduce coupling in both the forward and backward directions.**

I. INTRODUCTION

There is a rapidly expanding market for Si Microwave/Millimeter-Wave Integrated Circuits (MMICs) fabricated in standard CMOS foundries to replace GaAs MMICs in wireless communication systems, phased array radar, and other applications where the circuit cost is a major factor in determining the system cost. However, microwave passive elements and transmission lines placed directly on standard CMOS and BiCMOS grade Si, which have resistivities of 1 and 20 Ω-cm respectively, have low quality factors (high attenuation), which necessitates novel transmission line structures [1] that are typically embedded in polyimide that is deposited over the Si substrate. Moreover, highly integrated systems that include the RF circuits, digital data processing circuits, and bias control circuits on a single chip or within a single package also rely on multiple layers of polyimide to construct three-dimensional circuits that are smaller than what would normally be possible.

Thin film microstrip (TFMS) embedded in polyimide solves the problem of high attenuation and smaller sized circuits, but closely spaced TFMS lines also increases the potential for high levels of coupling between lines. If the interline crosstalk is too high, the circuit characteristics are severely degraded. Prior papers on reducing coupling between microstrip lines built on Low Temperature Cofired Ceramic (LTCC) have shown that a roll of via holes placed between the two lines reduces coupling by 8 dB if the via holes are connected on the top and bottom by a strip and the ground plane respectively [2]. This shield has also been shown to reduce coupling between TFMS lines embedded in polyimide on Si substrates [3]. However, completely covering the Si wafer for the TFMS ground plane does not leave substrate area for the Si circuit components. Therefore, TFMS with finite width ground planes is a more realistic transmission line, and if the ground plane is greater than 3 to 5 times the strip width, acceptable attenuation is achieved [4].

In this paper, a systematic evaluation of the coupling between TFMS lines with finite width ground planes embedded in polyimide built upon CMOS grade Si is presented for the first time. This in depth characterization includes a comparison of the coupling between transmission lines built on different layers of polyimide, and the use of metal filled via posts to connect ground planes on different layers. To characterize the coupling, Finite Difference Time Domain (FDTD) and measurements are used.

II. CIRCUIT DESCRIPTION

Figure 1 shows a cross sectional cut through microstrip lines embedded in polyimide upon a Si substrate. TFMS lines are characterized with ground plane widths of 3 and 5 times the strip width. W1, W2, and W3 are 23 μm, 52 μm, and 25 μm respectively to yield 50 Ω transmission lines for the polyimide thickness, h, of 10 μm. In several coupled microstrip lines, the two ground planes on different layers are connected by a single roll of 20 by 20 μm via holes spaced 100 μm apart. The parameter C is the distance between the center lines of the two microstrip lines.

A four-port circuit is used for characterizing the coupling between the microstrip lines with probe pads orientated so that each port may be probed simultaneously and the port numbering as shown in Figure 2. The coupling region, or the section of parallel transmission lines labeled L in Figure 2, is 5000 μm long for the experimental characterization, but the coupling length was varied for the FDTD analysis.

0-7803-7239-5/02/$10.00 © 2002 IEEE

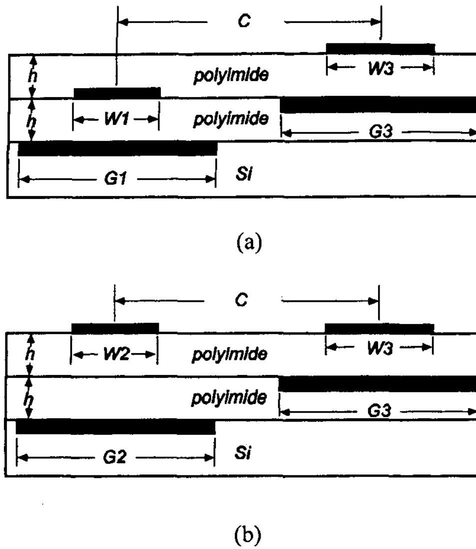

Figure 1: Cross sectional cuts through microstrip lines with finite width ground planes embedded in polyimide layers (a) microstrip lines with same substrate thickness (b) microstrip lines with different substrate thickness.

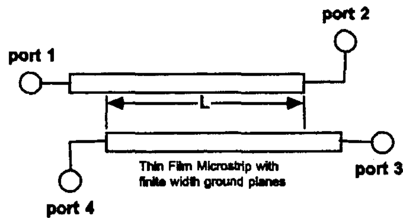

Figure 2: Schematic of the four-port microstrip line structure used to characterize coupling.

III. THEORETICAL ANALYSIS

The full-wave FDTD technique [5] is used for the theoretical characterization of the forward and backward coupling, S_{31} and S_{41} respectively, between the two parallel microstrip lines. The E- and H-field components are implemented in a leapfrog configuration. An adaptive grid with neighboring cell aspect ratio smaller or equal to 2 maintains a second-order global accuracy.

Numerical meshes of 80-120 by 45 by 250 cells terminated with 10 Perfectly Matched Layer (PML) cells in each direction provide accurate results for a time-step of $\Delta t=0.99\Delta t_{max}$. A Gaussian pulse with f_{max}=60GHz is applied vertically as a soft source close to the front end of the microstrip, and its values get superimposed on the FDTD calculated field value for all cells in the excitation region for each time-step. The via holes are modeled as rectangular metal tubes with cross-section 23x20 μm. To account for the excitation of different modes in the microstrip lines, two simulations are performed for each geometry exciting both lines with equal amplitude and even or odd space distributions respectively. In addition, both microstrip lines are terminated with matched loads (Z_o=50 Ω) that are realized as the combination of shunt resistors placed between the microstrip and the bottom ground [6]. Two probes placed at the front end and at the far end of one line are used for the combination of the results of the even and of the odd simulations. The application of the FFT algorithm derives the frequency-domain results from the time-domain data (usually 20,000 time-steps).

IV. CIRCUIT FABRICATION AND CHARACTERIZATION

The four port microstrip circuits are fabricated on a 1 Ω-cm Si wafer. A ground plane consisting of a 300 Å Ti adhesion layer, 1.5 μm of Au, and a 200 Å Cr cap layer is first evaporated onto the Si wafer. This is followed by spinning on Dupont adhesion promoter and 10 μm of Dupont PI-2611 polyimide, which has a permittivity of 3.12 measured at 1 MHz [7] and a loss tangent of 0.002 measured at 1 kHz [8]. After curing the polyimide at 340 C for 120 minutes, Ni is evaporated onto the polyimide to serve as a mask for the O_2/CF_4 reactive ion etching (RIE) of the via holes. After the via holes are etched and the Ni removed, 200 Å of Ti and 2000 Å of Au are sputtered onto the wafer to serve as a seed layer for the 1.3 μm of Au electroplating that is used to define the embedded microstrip lines and fill the via holes in a single step. This Au is capped with 200 Å of Cr before applying the next layer of polyimide. Thus, all metal structures are 1.5 μm thick. This process is repeated for each layer of polyimide. After each step, a DEKTAK surface profile is used to measure the polyimide and metal strip thickness. Both, the DEKTAK and SEM analysis show that the surface roughness is low enough that it can be neglected in the analysis.

Measurements are made on a vector network analyzer from 1 to 50 GHz. A Thru/Reflect/Line (TRL) calibration is implemented with MULTICAL [9], a TRL software program, using four delay lines of 1800, 2400, 4800, and 10000 μm and a short circuit reflect fabricated on the same substrate as the circuits. To improve accuracy, each circuit is measured several times and the average of those measurements is presented in this paper. During the measurement of the four-port circuits, two of the four

ports are terminated in 50 Ω loads built into especially designed RF probes.

V. MICROSTRIP COUPLING RESULTS

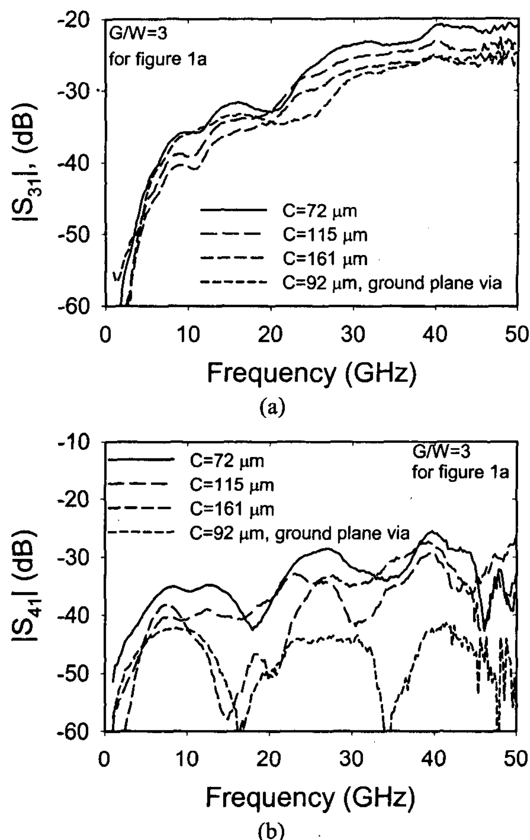

Figure 3: Measured S-parameters for coupled microstrip lines with the same substrate thickness (Figure 1a) as a function of frequency (a) forward coupling and (b) backward coupling.

First, the measured and FDTD analysis results for the embedded microstrip lines were compared across the frequency band of 1 to 50 GHz; the agreement was found to be very good with a difference less than 3 dB, thus allowing the derivation of conclusions from either method. A set of measured S-parameters for the coupled microstrip lines of Figure 1a is shown in Figure 3. Typical of all of the results presented in this paper, $|S_{31}|$ increases monotonically with frequency as shown in Figure 3a, and the slight variations in $|S_{31}|$ with frequency are shown by the FDTD analysis to be artifacts of the measurement setup. Without the ground plane via posts, $|S_{41}|$, increases with frequency, but there is also a periodic component that the FDTD analysis proves to be dependent on the coupling length, L. This is an indication that there are two components of coupling, direct coupling and indirect coupling through a phantom circuit or a parasitic mode [10]. When the ground planes are connected by via posts, $|S_{41}|$ is periodic with frequency and all of the peaks are at the same level, which is typical for coupled line structures. Throughout the rest of the paper, presented results are backward coupling defined as $-20*\log|S_{41}|$ and forward coupling defined as $-20*\log|S_{31}|$.

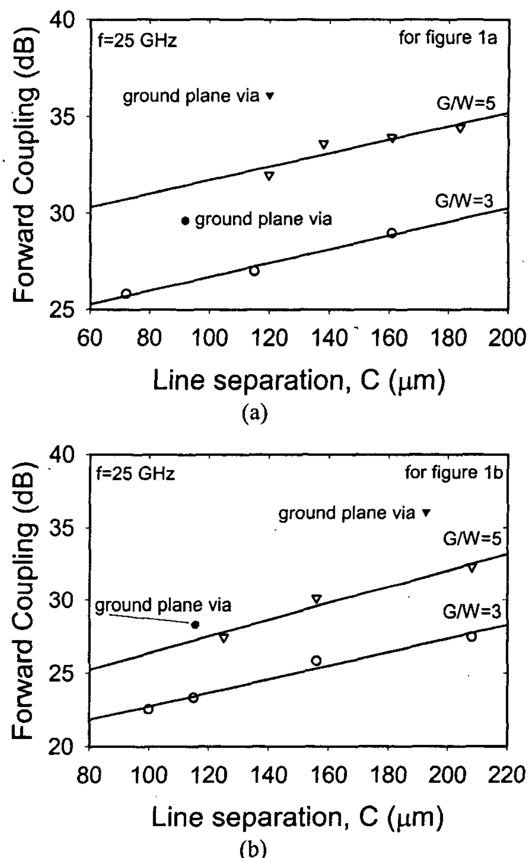

Figure 4: Measured forward coupling at 25 GHz of microstrip lines with (a) the same substrate thickness and (b) different substrate thickness as a function of center to center spacing, C.

The measured forward coupling for all of the lines is summarized in Figure 4. It is seen that coupling decreases as C increases, but the dependence is weak, especially compared to the coupling of TFMS with infinite ground planes presented in [3]. Furthermore, the forward coupling of the finite width ground plane TFMS is approximately 5 dB higher for small C and 10 dB higher for large C when compared to the infinite ground plane TFMS [3]. It is seen in Figure 4 that coupling decreases as the ground plane

width is increased. In Figure 4, the forward coupling for finite width ground plane TFMS with the ground planes connected by via posts is also shown, and it is seen that connecting the ground planes reduces coupling by 5 dB, which puts it at the same level measured for the infinite ground plane TFMS.

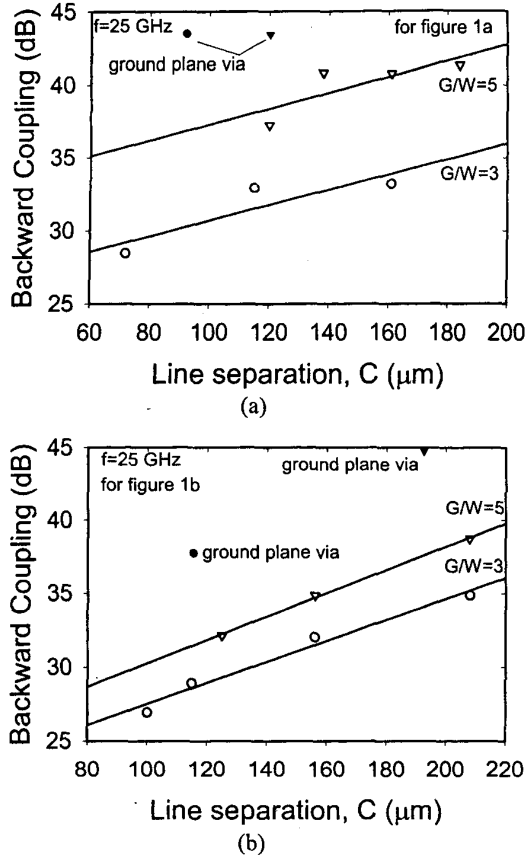

Figure 5: Measured backward coupling at 25 GHz of microstrip lines with (a) the same substrate thickness and (b) different substrate thickness as a function of center to center spacing, C.

The backward coupling measured at 25 GHz is summarized in Figure 5. Again, the coupling decreases as C increases as expected, but the dependence is weak compared to the infinite ground plane results [3]. Furthermore, the backward coupling is approximately 10 dB higher than the infinite ground plane TFMS, and the backward coupling decreases as the ground plane width is increased. When the ground planes of the two lines are connected by via posts, the backward coupling is reduced by 8 dB, yielding coupling that is approximately the same as the infinite ground plane TFMS.

VI. CONCLUSION

In this paper, we have characterized the coupling between microstrip lines with finite width ground planes embedded in polyimide layers on a low resistivity Si wafer. It is shown that the coupling is higher than for infinite width ground plane TFMS, but that similar coupling can be achieved if the two ground planes are connected by metal filled via posts. It is also shown that there is a large dependence in coupling on the ratio of the ground plane width to the strip width. Thus, although narrow ground planes may be used in 3D-MMICs, the circuit design must account for the higher coupling.

REFERENCES

[1] G. E. Ponchak, "RF transmission lines on silicon substrates," *29 th European Microwave Conference Dig.*, Munich, Germany, Oct. 5-7, 1999, pp. 158-161.

[2] G. E. Ponchak, D. Chun, J.-G. Yook, and L. P. B. Katehi, "The use of metal filled via holes for improving isolation in LTCC RF and wireless multichip packages," *IEEE Trans. on Advanced Packaging*, Vol. 23, No. 1, pp. 88-99, Feb. 2000.

[3] G. E. Ponchak, E. M. Tentzeris, and J. Papapolymerou, "Coupling between microstrip lines embedded in polyimide layers for 3D-MMICs on Si," *2001 IEEE MTT-S Int. Microwave Symposium Dig.*, Phoenix, AZ, May 20-25, 2001, pp. 1723-1726.

[4] G. E. Ponchak, A. Margomenos, and L. P. B. Katehi, "Low loss, finite width ground plane, thin film microstrip lines on Si wafers," *IEEE 2000 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems Dig.*, Garmisch, Germany, April 26-28, 2000, pp. 43-47.

[5] A. Taflove, *Computational Electrodynamics*, Artech House, Dedham, MA, 1995.

[6] L. Roselli, E. Tentzeris and L. P. B. Katehi, "Nonilnear circuit characterization using a multiresolution time domain technique," *Proc. of the 1998 MTT-S Conference*, pp.1387-1390, Baltimore, MD.

[7] J. Leu, H.-M. Ho, J. K. Lee, J. Kasthurirangan, C. N. Liao, and P. S. Ho, "The evaluation of low dielectric constant materials for deep submicron interconnect applications," in *Proc. 6th Meeting Dupont Symp. Polyimide Microelectronics*, May 1-3, 1995.

[8] Dupont Company Pyralin LX data sheet.

[9] R. B. Marks, "A multilane method of network analyzer calibration," IEEE Trans. Microwave Theory Tech., Vol. 39, pp. 1205-1215, July 1991.

[10] S. A. Schelkunoff and T. M. Odarenko, "Crosstalk between coaxial transmission lines," *Bell System Technical Journal*, Vol. 16, pp. 144-164, 1937.