

W-Band Finite Ground Coplanar Monolithic Multipliers

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Abstract—This paper describes the design, fabrication, and experimental evaluation of *W*-band planar monolithic varactor frequency multipliers based on finite ground coplanar (FGC) lines. These lines are a low-loss low-dispersion alternative of a planar transmission line to more conventional microstrip or coplanar waveguide lines at millimeter-wave frequencies. The near transverse-electromagnetic nature of propagation of the FGC lines simplifies circuit design and layout. Two-diode *W*-band varactor multipliers with input Q 's of two and three and FGC input and output have been realized. The multiplier with input $Q = 2$ has an output power of 72 mW, an efficiency of 16.3% near 80 GHz, and a -3 -dB bandwidth greater than 10 GHz, while the multiplier with $Q = 3$ has an efficiency of 21.5% near 70 GHz and a 6-GHz bandwidth. This paper will briefly describe the characteristics of the FGC lines, the design of the multipliers, and their radio-frequency performance.

Index Terms—Doubler, MMIC, planar circuit, Schottky diode.

I. INTRODUCTION

LOCAL oscillator sources are an important part of all high-frequency receivers. Transistor sources are available at lower frequencies and two-terminal devices such as Gunn oscillators provide power up to about 150 GHz, but harmonic multipliers are the main radio-frequency (RF) sources at higher frequencies. A detailed summary and review of multiplier performance can be found in [1] and [2]. Most multipliers are based on Schottky barrier diodes with early multipliers using a honeycomb anode chip with a whisker contact across a waveguide mount. Whisker-contacted diodes have very low parasitics, but they are difficult to handle, can have problems with thermal cycling and vibrations, and have performance that is critically dependent on the shape of the whisker. Even with these problems, whisker-contacted multipliers were the most common millimeter- and submillimeter-wave sources until the late 1980's. A typical low-power whisker-contacted multiplier had 35% efficiency at 98 GHz [3]. In 1987, Bishop *et al.* proposed the microchannel structure as an alternative high-frequency planar diode [4]. This structure was much easier to handle and could also be used to fabricate multiple diodes for the same mount. An example of this type of multiplier

is given by Rizzi *et al.* [5] and has a peak output power of 55 mW at 174 GHz and a peak efficiency of 25% using a balanced combination of two diode pairs. More recently, Erickson [6] has demonstrated a fixed tuned planar four-diode doubler centered at 150 GHz that has a 28% peak efficiency, 3-dB bandwidth of 130–168 GHz, and output power of 25–40 mW. Planar diodes are approaching the performance of their whisker counterparts.

Most millimeter-wave multipliers are based on waveguide circuits. Waveguide circuits have the low loss and high Q needed for efficient multiplier operation and can also include tuners and backshorts needed to optimize for peak performance. However, waveguide mounts are complex and become more difficult and expensive to machine with increasing frequency and smaller size. An alternative approach uses many diodes and quasi-optical techniques to greatly increase the power output [7]–[8]. This approach allows the power generation and tuning to function on a spatial grid with each grid element having printed tuning elements. The result is usually increased power and reduced efficiency when compared with waveguide multipliers. Another multiplier approach is monolithic or monolithic-microwave integrated-circuit (MMIC) multipliers. Many similar MMIC multipliers can be fabricated at the same time using integrated circuit (IC) fabrication techniques and, thus, producing low-cost circuits. However, planar circuits tend to have higher loss and lower Q when compared to waveguide ones and it is also more difficult to include tuning elements. Even with these limitations, some very useful MMIC multipliers have been reported. Chen *et al.* [9] described a planar MMIC multiplier with an output power of 65 mW and an efficiency of 25% at 94 GHz using a microstrip circuit.

This paper will describe the design, fabrication, and evaluation of *W*-band planar multipliers using a modified form of coplanar waveguide (CPW) lines. Preliminary results can be found in [10]. Section II will describe the properties of the new line structure. Section III will discuss the design and fabrication of the multipliers and Section IV will present the experimental results. The conclusions are summarized in Section V.

II. FGC LINES

Microstrips and CPW's are two guiding structures that are used extensively for high-frequency MMIC applications because of their planar geometry and compatibility with solid-state devices. However, microstrip characteristics depend on the substrate thickness and moding can occur at high frequencies unless the substrate is thinned. CPW is less dependent

Manuscript received July 17, 1998; revised November 11, 1998. This work was supported by Texas Instruments Incorporated, by the NASA Center for Space Terahertz Technology, and by the NASA Jet Propulsion Laboratory.

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Publisher Item Identifier S 0018-9480(99)03132-4.

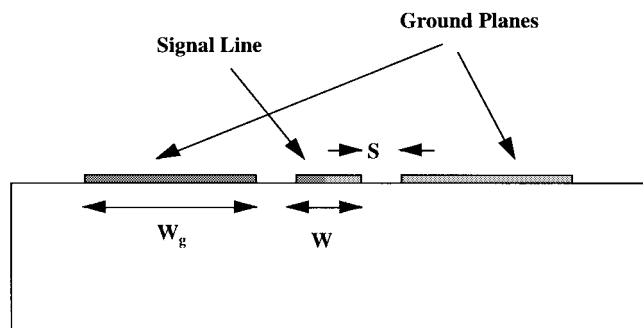


Fig. 1. FGC line geometry.

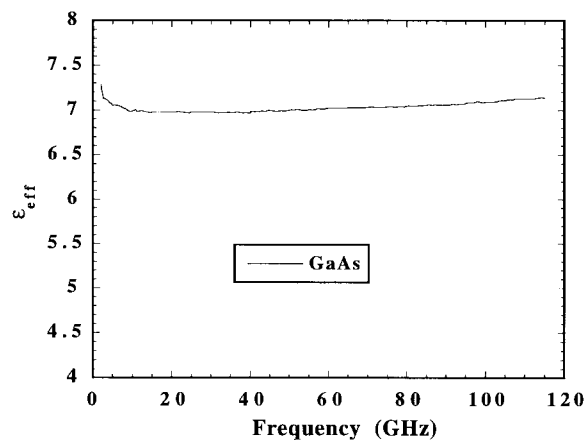
on the substrate thickness, but problems can occur because of parasitic parallel-plate waveguide modes. These modes can be suppressed with via holes that make circuit fabrication more difficult and can cause additional problems if placed incorrectly. The more complex propagation properties add to circuit-design problems since complicated line models are needed to correctly predict results. This paper proposes the use of a modified CPW structure with finite-width ground planes. This finite ground coplanar (FGC) line overcomes many of the problems associated with conventional CPW's and microstrip lines, and can be scaled easily to higher frequencies. A detailed description of these lines is given in [11].

The geometry of an FGC line is shown in Fig. 1. The narrow ground planes reduce the effect of parallel-plate modes, thus eliminating the need for via holes. Wafer thinning is not required, backside metallization does not affect the line characteristics and the loss is mainly ohmic and dependent on the geometry rather than the substrate material [12]. The FGC line supports two modes of operation to dc: the CPW and the coupled slot-line mode. However, the latter can be successfully suppressed by using symmetry around the center conductor or air-bridges. In a real application, where the circuit will be mounted on a metal carrier or package, the presence of the ground plane can excite the first parasitic microstrip mode. It has been found [14] that a single mode of operation is possible (cutoff frequency of first parasitic mode much higher than band of operation) if the line geometry is chosen so that the width of the entire structure is less than half the wavelength in the dielectric at the highest operating frequency. Correct selection, therefore, of the FGC line geometry is fundamental for the minimization of parasitic-mode effects in any real circuit.

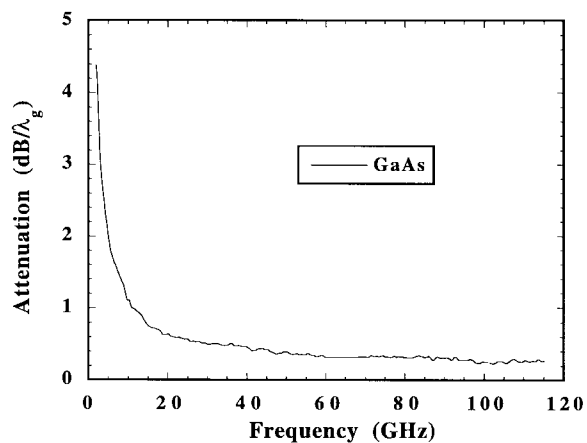
A quasi-static solution of Laplace's equation using a finite-element solver¹ and a conformal point-matching method [13] were used to characterize these lines. These codes are very fast and were used to predict useful geometries for fabrication. Several representative structures were then fabricated and measured. The ground strip width must be narrow to avoid moding and wide enough to reduce loss. An extensive set of measurements by Ponchak [14] indicates that the ground width should be

$$W_g \approx s + 2w \quad (1)$$

where the dimensions are defined in Fig. 1. Test lines were fabricated on 500- μm -thick GaAs substrates using a 500- \AA -thick Ti adhesion layer and 1- μm -thick gold conductors. The



(a)



(b)

Fig. 2. Measured FGC properties. (a) Effective dielectric constant versus frequency. (b) Loss versus frequency.

total line width was 460 μm , corresponding to a higher order mode cutoff frequency of approximately 180 GHz. The width w of the signal conductor was 50- μm while the slot width s was 45 μm for this test line. The lines were measured from 2 to 60 GHz and 70 to 118 GHz using an Alessi probe station with different probes for each frequency band and a measurement system that was calibrated using the NIST MultiCal program [15].² The measured loss and dielectric constant of the lines are shown in Fig. 2. The approximately constant permittivity indicates low dispersion and a nearly pure transverse electromagnetic (TEM) mode propagation over the entire frequency range. The loss normalized to the guided wavelength has an inverse square-root dependence, indicating that it is mainly ohmic. The loss is approximately 0.23 dB/ λ_g at 100 GHz.

A variety of filters, stubs, and line steps were investigated in order to obtain information on building blocks needed for the multipliers. The details of these results are given in [11]. Parallel stubs were used for the multipliers in this paper, thus, their characteristics will be described. A photograph of a planar open stub with two 1440- μm -long stubs and 20- μm signal lines and slots is shown in Fig. 3(a). The lines have air-bridges at the corners and the junctions to equalize the ground planes and suppress the coupled slot-line mode. The 50- Ω feed lines

¹PDease, Macsyma, Arlington, MA.²R. Marks and D. Williams, Program MultiCal, rev. 1.00 NIST, Aug. 1995.

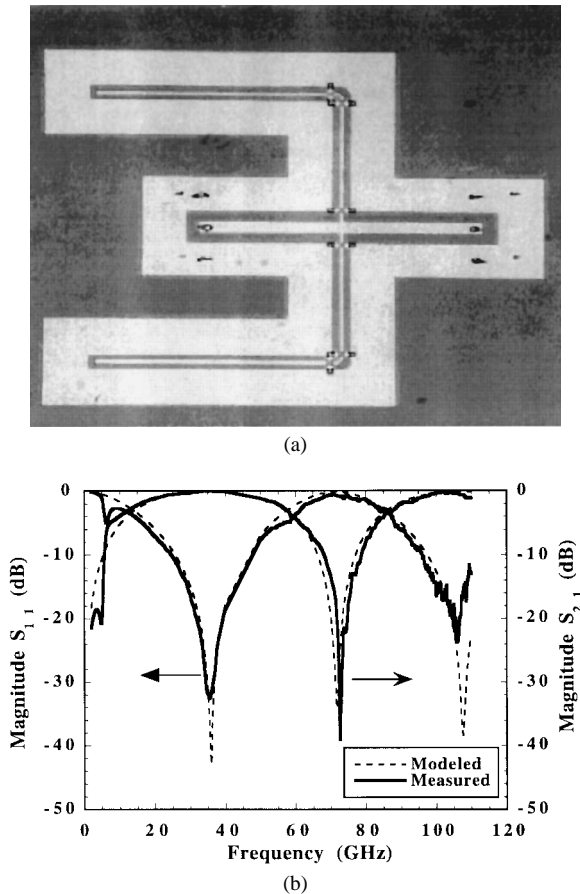


Fig. 3. Planar open stub. (a) Photograph. (b) Measured and fitted return and insertion loss from 2 to 110 GHz.

have the same dimensions as the test line described in the above paragraph. The measured data were fitted to a lossy TEM transmission-line model using LIBRA. A comparison of the modeled and measured results is shown in Fig. 3(b). There is a close fit between the measured and simulated results, again indicating that the FGC line can be correctly described by a nondispersive lossy TEM line model, which can be used to easily and accurately design the passive circuitry around the multiplier diodes. The model did not include any additional elements for the junction. Similar stubs were used as input and output filters on the multipliers.

III. MULTIPLIER DESIGN

FGC line elements with characteristic impedances varying from 20 to 80 Ω were used as a starting point for the multiplier design. A nonlinear multiple-reflection program that includes velocity saturation, forward conduction, and avalanche breakdown, modified from the code described by East *et al.* [16], was used to design the multipliers. The varactor diode is usually specified and the multiplier is designed around it in conventional multiplier design. Here, the diode parameters become part of the design process; the operating frequency sets the doping level and the peak RF voltage swing limited by the breakdown voltage set the active epitaxial layer width. Multiplier operation varies from a resistive mode where the current is dominated by conduction current to a reactive or varactor mode where the current is dominated by the pumping of the depletion layer capacitance. The diode input Q is a

TABLE I
MEASURED DC CHARACTERISTICS FOR THE FABRICATED DIODES

R_S (Ω)	C_{jo} (fF)	η	I_o (fA)	V_{BR} (V)	f_C (GHz)
2.2	88	1.15	185	-11.8	822

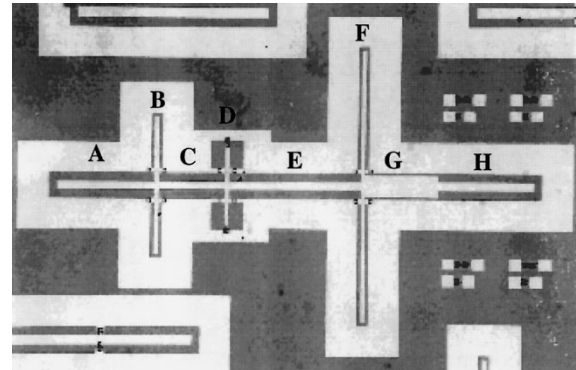


Fig. 4. Fabricated multiplier based on FGC line technology.

measure of the operating mode. Resistive or low Q multipliers have modest efficiencies and wide bandwidths, while reactive multipliers have higher efficiencies and smaller bandwidths. The impedances in high Q circuits are more sensitive to small variations in the dimensions of the lines in the experimental circuits. High Q multipliers also have a larger RF voltage swing across the active device than a lower Q multiplier, for a given available pump power. This limits the pump power in high Q multipliers [16]. Waveguide multipliers can be designed for higher Q , with modest differences in the design versus realized impedances adjusted with tuners and backshorts. Similar impedances in a MMIC multiplier are fixed, with the bias point being the only available "tuning." The multiple reflection code was modified to adjust the diode area and bias so that the required embedding impedances could be realized for designs with diode input Q 's of two and three. The $Q = 2$ diodes had an epitaxial layer doping of $10^{17}/\text{cm}^3$, a thickness of 4700 \AA , and an area of $63 \mu\text{m}^2$ per diode with a bias tuning voltage of -3.5 V, whereas the $Q = 3$ diodes had an epi-layer thickness of 4000 \AA and an area of $66 \mu\text{m}^2$ per diode with a bias tuning voltage of -6.5 V. The difference of the epi-layer thickness between the two diodes is due to the different material that was available at the time of fabrication. It should be noted here that there is no fundamental difference between the $Q = 2$ and $Q = 3$ diodes, except for the bias voltage. The dc parameters for the diodes can be found in Table I. The single-diode input impedance was $51.5-j106 \Omega$ and $52.4-j160.8 \Omega$ for the $Q = 2$ and $Q = 3$ diode, respectively, at the fundamental frequency. The multiplier circuit, designed for an 80-GHz output frequency, was printed on a GaAs semi-insulating wafer after the doped active layer was etched away.

IV. EXPERIMENTAL RESULTS

A variety of multipliers, including series and shunt configurations and single- and multiple-diode structures, were designed, fabricated, and tested. The best results, which were obtained with the diode-pair shunt structure, will be described here. The details on the other multipliers are given in [17]. The $Q = 2$ multiplier shown in Fig. 4, is designed with 50- Ω

TABLE II
GEOMETRICAL CHARACTERISTICS FOR THE $Q = 2$ MULTIPLIER

Section	Section Description	w (μm)	s (μm)	Length (μm)
A	50 Ω signal launch structure	50	45	500
B	Open-end balanced stub	20	20	331
C	50 Ω standard section	50	45	354
D	Diode feed lines (short end stub model)	20	80	213
E	50 Ω standard section	50	45	709
F	Open-end balanced stub	20	20	682
G	Low impedance section	120	10	380
H	Signal launch structure	50	45	500

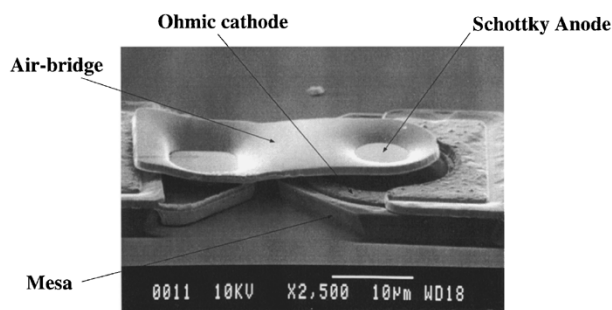


Fig. 5. SEM photograph of the Schottky barrier diode.

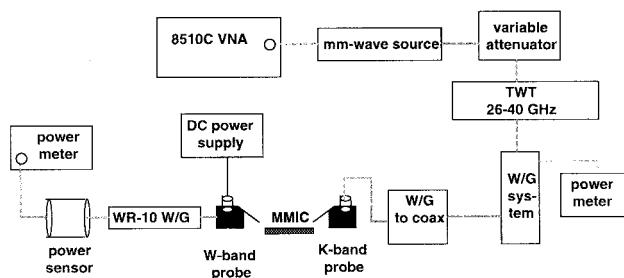


Fig. 6. Block diagram of measurement system setup.

input and outputs on the ends, a second harmonic trap on the input side, and a fundamental trap on the output side. The varactor diodes are connected to the main line with inductive lines that cancel out the average capacitance of the diodes. Additional information about the structure is given in Table II and a close-up photograph of the diode is shown in Fig. 5.

The multiplier was evaluated using on-wafer probing at the input and output. The input and output measurements were calibrated to the tips of the probes using *Ka*-band and *W*-band HP 8510 test sets and power meters at the pump and output frequencies. A *Ka*-band traveling-wave tube (TWT) was used as the source. This combination of input and output test-set frequencies limited the output frequency range from 66 to 80 GHz. The details of the calibration and error correction are given in [17] and a block diagram of the measurement system can be seen in Fig. 6. The measured output power and efficiency of the $Q = 2$ multiplier are shown in Fig. 7. The peak efficiency was 16.3% and the peak output power was 72 mW at 80 GHz. The design worked well over the entire

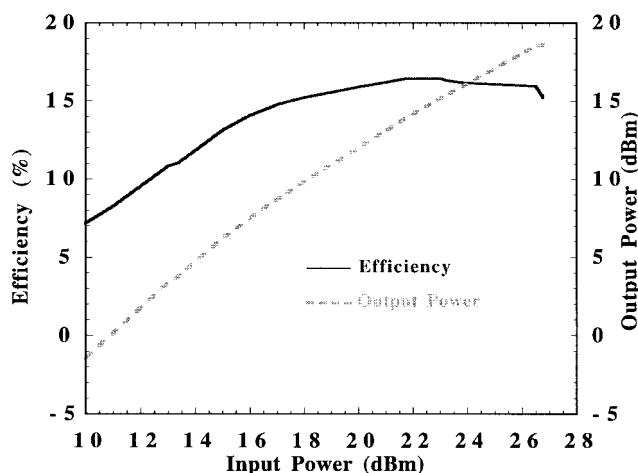


Fig. 7. Output power and efficiency versus input power for the $Q = 2$ multiplier at 80 GHz.

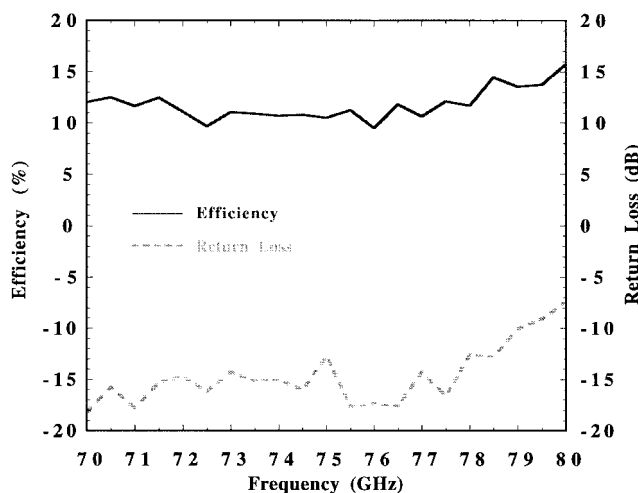


Fig. 8. Efficiency and return loss versus frequency for the $Q = 2$ multiplier for a constant input power level of 20 dBm.

measurement frequency range. The efficiency and return loss from 70 to 80 GHz for a constant 20-dBm input power are shown in Fig. 8. The -3 -dB efficiency bandwidth is wider than the 10-GHz measurement bandwidth. A second iteration of this multiplier had an output power of 93 mW at 71.5 GHz,

TABLE III
GEOMETRICAL CHARACTERISTICS FOR THE $Q = 3$ MULTIPLIER

Section	Section Description	w (μm)	s (μm)	Length (μm)
A	50 Ω signal launch structure	50	45	500
B	Open-end balanced stub	50	19	346
C	50 Ω standard section	50	45	360
D	Diode feed lines (short end stub model)	20	80	268
E	50 Ω standard section	50	45	702
F	Open-end balanced stub	20	20	682
G	Low impedance section	120	10	307
H	Signal launch structure	50	45	500

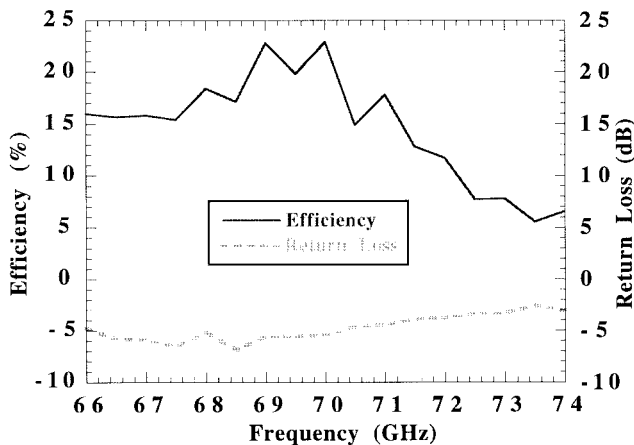


Fig. 9. Efficiency and return loss versus frequency for the $Q = 3$ multiplier for a constant input power level of 17 dBm.

but with a lower efficiency. The design efficiency of this multiplier was 33%. The estimated loss of the input and output circuits based on line measurements was 1.1 dB and the return loss at the peak efficiency point was -7.5 dB. The resulting multiplier internal efficiency is 26%, in reasonable agreement with the model prediction. This output power level is among the best reported for MMIC multipliers at W -band.

For the $Q = 3$ multiplier, the dimensions of the different stubs and line sections can be seen in Table III and the measured results in Fig. 9. The peak efficiency was 21.5% at 70 GHz and the -3 -dB bandwidth was approximately 6 GHz. The design efficiency for this multiplier was 39%. The input power level for the $Q = 3$ multiplier was 17 dBm, in contrast with the $Q = 2$ multiplier where the input level was 20 dBm. For higher input power levels, the efficiency of the $Q = 3$ multiplier was less than 21.5%. This is expected since, for higher Q 's, the RF voltage swing across the diode increases, leading to increased saturation effects in the device and limiting the maximum input power before burn out. The $Q = 3$ doubler also has a smaller bandwidth than the $Q = 2$ since both the diode and embedding impedances vary more rapidly with frequency, mismatching the input pump power. Thus, higher Q multipliers can achieve more efficiency with less bandwidth than lower Q 's, but at smaller input power levels, resulting in smaller output power due to the saturation effects

[16]. Comparing the experimental results of the $Q = 2$ and 3 multipliers with those of [6], the lower efficiency is expected since the planar circuits are much lossier than the waveguide ones and the diodes are different (four instead of two).

V. CONCLUSIONS

This paper describes the design, fabrication, and evaluation of W -band multipliers using FGC lines. These lines overcome many of the problems associated with traditional planar transmission lines at millimeter- and submillimeter-wave frequencies, such as the microstrip and CPW line. They have very low dispersion and loss compared to those lines, and allow circuit design using simple TEM line element models. They can also be scaled easily to much higher frequencies with little additional fabrication complexity. A $Q = 2$ W -band multiplier designed using these lines had an efficiency of 16.3%, output power of 72 mW, and -3 -dB output frequency range wider than 10 GHz, while a $Q = 3$ multiplier had a 21.5% efficiency at 70 GHz with 6-GHz bandwidth. Work is currently under way for the fabrication of a monolithic doubler centered between 170–180 GHz.

ACKNOWLEDGMENT

The authors would like to thank Dr. S. Robertson, The University of Michigan at Ann Arbor, for help with this paper.

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